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Docket No.: M4065.0415/P415
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kie Y. Ahn et al.

Application No.: 09/755,071 Group Art Unit: 2815

Filed: January 8, 2001 Examiner: G. C. Eckert

For: COPPER DUAL DAMASCENE
INTERCONNECT TECHNOLOGY

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is responsive to the Notification of Non-Compliant Appeal Brief dated December 1, 2004. Enclosed is an Appellants' Amended Brief on Appeal (29 pages) for filing in connection with the above-referenced patent application. The Amended Brief is responsive to the December 1, 2004 Notification and is different from the original Brief in the following aspects:

1. The Amended Brief lists the items required under 37 C.F.R. § 41.37(c) under the proper heading and order;

2. The Summary of Claimed Subject Matter refers to the specification by page and line number, and to the drawings by reference characters; and

3. The Amended Brief contains a concise statement of each ground of rejection presented for review.

The Amended Brief is believed to be in full compliance with 37 C.F.R. § 41.37.

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0415/P415.

Dated: January 3, 2005

Respectfully submitted,

By _____

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Docket No.: M4065.0415/P415
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kie Y. Ahn et al.

Application No.: 09/755,071 | Confirmation No.: 5118

Filed: January 8, 2001 | Art Unit: 2815

For: COPPER DUAL DAMASCENE INTERCONNECT TECHNOLOGY | Examiner: Eckert II, George C.

APPELLANTS' AMENDED BRIEF ON APPEAL

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Amended Brief for an appeal pursuant to 35 U.S.C. § 134 and 37 C.F.R. § 41.31 et seq. from the final rejection of claims 19-28, 30, 31, 33, 34, 37 and 39-42 of the above-identified application (the "Application") mailed March 22, 2004. The Notice of Appeal was filed on July 19, 2004 with one month extension of time. The original Appeal Brief was filed on September 20, 2004. The Notification of Non-Compliant Appeal Brief under 37 C.F.R. §41.37 was mailed on December 1, 2004. Any deficiency in the fees associated with this Amended Brief should be charged to our Deposit Account No. 04-1073.

This Amended Brief contains items under the following headings as required by 37 C.F.R. § 41.31:

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is MICRON TECHNOLOGY, INC., a Corporation of the State of Delaware, the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

An appeal known to Appellants which may affect the Board's decision in this appeal relates to copending U.S. Application Serial No. 10/392,178 filed on March 20, 2003 (Attorney Docket No. M4065.0415/P415-B). The Notice of Appeal in related copending U.S. Application Serial No. 10/392,178 was filed on August 12, 2004 and the Appellants' Brief on Appeal was filed on October 5, 2004.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 19 claims pending in this application.

Claims 19, 21, 22, 24, 25, 28 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand (U.S. Patent No. 6,362,528) in view of Min et al. in

Metal-organic atomic-layer deposition of titanium-silicon-nitride films, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999).

Claims 20, 23 and 40-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand (U.S. Patent No. 6,362,528) and Min et al. in *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999) and further in view of Venkatraman et al. (U.S. Patent No. 6,093,966).

Claims 26 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand (U.S. Patent No. 6,362,528) and Min et al. in *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999) and further in view of Reid et al., *Ti-Si-N Diffusion Barriers Between Silicon and Copper*, IEEE Electron Devices Lettrs., Vol. 15, No. 8, pp. 298-300 (1994).

Claims 31, 33, 34, 37 and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand (U.S. Patent No. 6,362,528) in view of Venkatraman et al. (U.S. Patent No. 6,093,966) and Reid et al., *Ti-Si-N Diffusion Barriers Between Silicon and Copper*, IEEE Electron Devices Lettrs., Vol. 15, No. 8, pp. 298-300 (1994).

B. Current Status of Claims

1. Claims canceled: 1-18, 29, 32, 35, 36 and 38

2. Claims withdrawn from consideration but not canceled: none

3. Claims pending: 19-28, 30, 31, 33, 34, 37 and 39-42

4. Claims allowed: none

5. Claims rejected: 19-28, 30, 31, 33, 34, 37 and 39-42

C. Claims On Appeal

The claims on appeal are claims 19-28, 30, 31, 33, 34, 37 and 39-42.

IV. STATUS OF AMENDMENTS

Appellants filed an Amendment After Final Rejection on December 10, 2003. The Examiner responded to the Amendment After Final Rejection with another final Office Action dated March 22, 2004. In the March 22, 2004 final Office Action, Examiner Eckert indicated that Appellants' proposed amendments to claims 19, 31, 40 was entered. Examiner Eckert also indicated that claims 35 and 36 were canceled and that newly added claim 42 was entered. Subsequent to the March 22, 2004 final Office Action, Appellants conducted a personal interview with Examiner Eckert on June 25, 2004. A Notice of Appeal was filed on July 19, 2004. No amendments have been submitted subsequent to the final Office Action dated March 22, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the discussion below, reference is made to the specification and drawings for exemplary embodiments of the invention covered by the claims. The specification and drawings references are not be considered as limiting the scope of the invention as defined by the claims.

The claimed invention relates to a copper damascene interconnect structure of a semiconductor device with reduced diffusion of copper atoms to underlying damascene layers. (Application at 4, lines 6-9). According to the claimed invention, the damascene interconnect structure may be part of a damascene structure that may be further part of an integrated circuit coupled with a processor-based system. (Application at 7, lines 10-13; Figure 14, reference character 100; Figure 16, reference character 200; Figure 17, reference character 300; Application at 13, lines 10-23; Figure 18, reference character 400).

Claims 19-28 and 30

According to claims 19-28 and 30 of the application, the dual damascene structure comprises *inter alia* "a semiconductor substrate," "a first insulating layer

provided over said semiconductor substrate," "a metal layer provided within said first insulating layer" and "a second insulating layer provided over said metal layer." (Application at 7, lines 13-28; at 8, lines 1-8; Figures 4-17; reference character 50, 51, 52, 55). The dual damascene structure of claims 19-28 and 30 also comprises "a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material." (Application at 8, lines 19-28; at 9, lines 19-29; at 10, lines 1-8; Figure 8, reference character 65; Figures 11-17, reference character 72). The dual damascene structure of the claimed invention further comprises "a third insulating layer located over said second insulating layer" and "a trench situated within said third insulating layer and extending to said via, said trench being lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material." (Application at 8, lines 9-18; at 9, lines 1-29; at 10, lines 1-8; Figures 6-17, reference character 57; Figure 10; reference character 67; Figures 11-17, reference character 72).

According to the claimed invention, copper is employed to fill in the trenches and vias. (Application at 10, lines 21-22; Figure 13, reference character 80; Figure 15, reference character 81). The copper may be either selectively deposited by a CVD process, or deposited by an electroless technique *in lieu* of the selective copper CVD process. (Application at 10, lines 21-29; at 11, lines 1-9; Figure 13, reference character 80; Figure 15, reference character 81). Either way, "the adhesion of copper atoms to the underlying layers is increased, while the diffusion of copper atoms into adjacent interconnect layers is suppressed." (Application at 4, lines 15-17).

Claims 31, 33, 34, 37 and 39

Claims 31, 33, 34, 37 and 39 recite a "damascene structure" that comprises *inter alia* "a semiconductor substrate," "a first insulating layer provided over said semiconductor substrate" and "a metal layer provided within said first insulating layer." (Application at 7, lines 13-18; Figures 4-17; reference character 50, 51, 52). Claims 31,

33, 34, 37 and 39 also recite "at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS." (Application at 7, lines 19-28; at 8, lines 1-18; Figures 5-17; reference character 55, 57).

Claims 31, 33, 34, 37 and 39 further recite "at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material." (Application at 8, lines 19-28; at 9, lines 1-29; at 10, lines 1-8; Figure 8, reference character 65; Figure 10; reference character 67; Figures 11-17, reference character 72; Application at 10, lines 21-22; Figure 13, reference character 80; Figure 15, reference character 81).

Claims 40 and 41

Claims 40 and 41 recite a "processor-based system" comprising "a processor" and "an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure." (Application at 13, lines 10-23; Figure 18, reference character 400, 448; Figure 14, reference character 100; Figure 16, reference character 200; Figure 17, reference character 300).

Claims 40 and 41 further recite that the damascene structure comprises "a metal layer provided within a first insulating layer formed over a substrate, at least another insulating layer provided over said metal layer, said first insulating layer and said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS" and "an etch stop layer provided between said first insulating layer and

said at least another insulating layer." (Application at 7, lines 13-28; at 8, lines 1-18; Figures 5-16; reference character 50, 51, 52; 55; 56; 57).

Claims 40 and 41 additionally recite "at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper." (Application at 8, lines 19-28; at 9, lines 1-13; Figure 8, reference character 65; Figure 10, reference character 67; Application at 9, lines 16-29; at 10, lines 1-20; Figure 11-17; reference character 72; Application at 10, lines 21-29; at 11, lines 1-9; Figure 13, reference character 80; Figure 15, reference character 81).

Claim 42

Claim 42 recites a "damascene structure" comprising *inter alia* "a first insulating layer provided over a semiconductor substrate," "a metal layer provided within said first insulating layer" and "at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS." (Application at 7, lines 13-28; at 8, lines 1-18; Figures 4-17; reference character 50, 51, 52; 55; 57).

Claim 42 also recites "an etch stop layer provided over and in contact with said at least another insulating layer." (Application at 8, lines 8-10; Figure 5-16; reference character 56). Claim 42 further recites "at least one opening situated within said at least another insulating layer and said etch stop layer, and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material." (Application at 8, lines 19-28; at 9, lines 1-13; Figure 8, reference character 65; Figure 10, reference character 67; Application at 9, lines 16-29; at 10, lines 1-20; Figure 11-17; reference character 72; Application at 10, lines 21-29; at 11, lines 1-9; Figure 13, reference character 80; Figure 15, reference character 81).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejections to be reviewed in this appeal are the following:

Claims 19, 21, 22, 24, 25, 28 and 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Anand (U.S. Patent No. 6,362,528) in view of Min et al., *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999).

Claims 20, 23, 40, 41 and 42 stand rejected under 35 U.S.C. § 103 as being unpatentable over Anand (U.S. Patent No. 6,362,528) and Min et al., *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999) and further in view of Venkatraman et al. (U.S. Patent No. 6,093,966).

Claims 26 and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Anand (U.S. Patent No. 6,362,528) and Min et al., *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999) and further in view of Reid et al., *Ti-Si-N Diffusion Barriers Between Silicon and Copper*, IEEE Electron Devices Lettrs., Vol. 15, No. 8, pp. 298-300 (1994).

Claims 31, 33, 34, 37 and 39 stand rejected under 35 U.S.C. § 103 as being unpatentable over Anand in view of Venkatraman et al. (U.S. Patent No. 6,093,966) and Reid et al., *Ti-Si-N Diffusion Barriers Between Silicon and Copper*, IEEE Electron Devices Lettrs., Vol. 15, No. 8, pp. 298-300 (1994).

VII. ARGUMENTS

A. CLAIMS 19, 21, 22, 24, 25, 28 AND 30 ARE PATENTABLE OVER ANAND ET AL. (U.S. PATENT NO. 6,362,528) IN VIEW OF MIN ET AL. (*METAL-ORGANIC ATOMIC-LAYER DEPOSITION OF TITANIUM-SILICON-NITRIDE FILMS*)

Claims 19, 21, 22, 24, 25, 28 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand (U.S. Patent No. 6,362,528) ("Anand") in view of Min et al., *Metal-organic atomic-layer deposition of titanium-silicon-nitride films*, Appl. Phys. Lettrs., Vol. 75, No. 11, pp. 1521-23 (1999) ("Min"). The final Office Action asserts that "Anand in view of Min teach the claimed structure and make obvious the instant claims." (March 22, 2004 Office Action at 2). Specifically, the Office Action asserts that "[r]egarding . . . claim 19, Min teaches a process which achieves a Ti-Si-N layer with a step coverage of approximately 100% which is also the motivation for using the process." (March 22, 2004 Office Action at 2).

The claimed invention relates to a damascene structure having a via lined with a titanium-silicon-nitride layer and filled with copper. As such, independent claim 19 recites a "dual damascene structure" comprising *inter alia* a "metal layer provided within [a] first insulating layer," "a second insulating layer provided over said metal layer" and "a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material." Independent claim 19 also recites a trench situated within a third insulating layer and "lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material."

Dependent claims 21 and 24 recite that the second insulating layer (claim 21) and the third insulating layer (claim 24) "includes silicon oxide," while dependent claims 22 and 25 recite that the second insulating layer (claim 22) and the third insulating layer

(claim 25) "has a thickness of about 2,000 to 15,000 Angstroms." Dependent claim 28 recites that the copper material "includes copper or copper alloy." Dependent claim 30 recites that the substrate is "a silicon substrate."

Anand relates to a "bonding pad . . . formed in a lattice-like shape." (Abstract). According to Anand, the bonding pad is "constituted by a conductive member filled in grooves made in an insulating layer having a flat surface." (Col. 7, lines 26-28). Anand also teaches "an etching stopper layer formed on the insulating layer and having an opening to expose the bonding pad" and "a passivation layer formed on the etching stopper layer and having an opening to expose the bonding pad." (Col. 7, lines 28-33).

Min relates to achieving "near-perfect step coverage" and "control[ling] precisely the thickness and composition of grown films" by metal-organic atomic-layer deposition. As emphasized by Min et al., "the MOALD (metal-organic atomic-layer deposition) process has great potential for excellent step coverage on severe surface topography due to the complete surface reaction," particularly for Ti-Si-N films with less than 10nm thickness. Id. at 1523.

1. Anand and Min do not teach or suggest the subject matter of claims 19, 21, 22, 24, 25, 28 and 30

The subject matter of claims 19, 21, 22, 24, 25, 28 and 30 would not have been obvious over Anand in view of Min. Indeed, the final Office Action failed to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, the final Office Action failed to establish all elements of a showing of a *prima facie* case of obviousness. Specifically, Anand and Min, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 19. Anand fails to disclose, teach or suggest a "dual damascene structure" comprising *inter alia* "a via situated within said second insulating layer . . . said via being lined with an *organo-metallic-atomic deposited titanium-silicon-nitride layer* . . . and filled with a copper material," as independent claim 19 recites (emphasis added). According to Anand, barrier metal 17a, which would arguably correspond to the organo-metallic-atomic deposited titanium-silicon-nitride layer, is formed "on the insulating layer 25, on an inner surface of the contact hole 16a and the inner surfaces of the grooves 16b *by the CVD method or PVD method*" and "is made of, for examples a lamination of titanium and titanium nitride, or silicon titanium nitride." (Col. 12, lines 7-12; Fig. 31) (emphasis added).

Appellants submit that the limitation "organo-metallic-atomic deposited titanium-silicon-nitride layer" is not a product-by-process limitation, as the final Office Action mistakenly asserted, but rather is a *resulting structure* having defined and distinct characteristics. In R2 Medical Systems, Inc. v. Katecho, Inc., which involved a claim reciting that one element be "affixed" to another, the Court found that "'affixed' means 'to be attached physically.'" R2 Medical Systems, Inc. v. Katecho, Inc., 931 F.Supp. 1397, 1425-26 (N.D. Ill. 1996). The Court held that "[t]he terms of the claims do not indicate that 'affixed' refers to a process by which the stannous chloride is bound to the conductive plate, but only that it refers to the result of that process." Id. (quoting CVI/Beta Ventures, Inc. v. Custom Optical Frames, Inc., 893 F. Supp. 508, 519 (D. Md. 1995) (limitation that element be in 'work-hardened pseudoelastic metallurgic state' is directed to the structure, not the process, of manufacture)).

In re Garnero involved a patent claim which recited "expanded perlite particles which are interbonded one to another by interfusion between the surfaces of the perlite particles while in a pyroplactic state to form a porous perlite material." In re Garnero, 412

F.2d 276 (CCPA 1969). The Court of Customs and Patent Appeals held that "interbonded . . . by interfusion" should be interpreted as a structural rather than a process limitation. Id.

Similarly, in Hazani v. U.S. Int'l Trade Comm'n, which involved patent claims to a memory cell comprising a conductive plate having a surface that was "chemically engraved," the Federal Circuit also held that the claims were "pure product claims" and not product-by-process claims. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473 (Fed. Cir. 1997). The Federal Circuit reasoned that the "chemically engraved" limitation, read in context, described the product more by its structure rather than by the process used to obtain it. Id.

In the present case, independent claim 19 recites the limitation "organo-metallic-atomic deposited titanium-silicon-nitride layer" which is a structural limitation and not a product-by-process limitation. An "organo-metallic-atomic deposited titanium-silicon-nitride layer," like the "chemically engraved" plate of Hazani, is a *resulting structure* having distinct and defined characteristics. Thus, in view of R2 Medical Systems and Hazani, the limitation "organo-metallic-atomic deposited titanium-silicon-nitride layer" is not a product formed by a particular process.

Appellants also submit that the specification of the present invention teaches the improved characteristics of the "organo-metallic-atomic deposited titanium-silicon-nitride layer." For example, the specification mentions that "Min et al. have demonstrated that Ti-Si-N films deposited by an organo-metallic atomic layer deposition (ALD) method prevent the diffusion of copper at temperatures up to 800°C for about 60 minutes." (Application at 9, lines 23-25). The specification also emphasizes that "[t]he Ti-N-Si films formed by the above-described ALD technique prevent the diffusion of copper at temperatures up to 800°C for about 60 minutes, and provide a step coverage of about 100%." (Application at 10, lines 3-5). In this manner, "[a]s the aspect ratio of via/trench increases, maintaining a good step coverage is particularly important for the Ti-Si-N diffusion barrier layer 72 deposited especially on the sidewalls of the via 65 and trench 67."

(Application at 10, lines 5-8).

Achieving "near-perfect step coverage" and "control[ling] precisely the thickness and composition of grown films" by metal-organic atomic-layer deposition is also the crux of Min, the disclosure of which was incorporated by reference in the present application. As emphasized by Min, "the step coverage on severe surface topography due to the complete surface reaction" particularly for Ti-Si-N films with less than 10nm thickness. Id. at 1523. Accordingly, a person skilled in the art would conclude that the properties of the Ti-Si-N film associated with the metal-organic deposition of the present invention are different from the properties of a Ti-Si-N film formed by chemical vapor deposition, for example. Thus, the limitation "organo-metallic-atomic deposited titanium-silicon-nitride layer" of independent claim 19 is a structural limitation and not a product-by-process limitation. An "organo-metallic-atomic deposited titanium-silicon-nitride layer," like the "chemically engraved" plate of Hazani, is a *resulting structure* having distinct and defined characteristics.

Appellants further submit that Anand is also silent about "a via . . . being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer *having a step coverage of about 100%*," as independent claim 19 recites (emphasis added). The crux of Anand is preventing dishing which occurs as a result of excessive etching of the bonding pad during CMP processing, and not achieving a good step coverage, much less achieving a good step coverage in damascene processing, as in the claimed invention. Anand specifically mentions that "[s]uch dishing easily causes a bonding error, that is, a wire cannot be bonded to the bonding pad . . . accurately during a wiring bonding operation, which results in the deterioration of the production yield." (Col. 3, lines 18-22). Thus, Anand fails to disclose, teach or suggest all limitations of independent claim 19.

Similarly, Min is silent about using the disclosed process to produce a dual damascene structure, much less about a "dual damascene structure" having "a metal layer provided within [a] first insulating layer," "a second insulating layer provided over said metal layer" and "a via situated within said second insulating layer and extending to at least

a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material," as independent claim 19 recites. For at least the reasons above, Anand and Min, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 19.

2. No suggestion or motivation to combine Anand with Min exists

Appellants also submit that a person of a person of ordinary skill in the art would not have been motivated to combine the teachings of Anand with those of Min. To establish a *prima facie* case of obviousness, "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573. This way, a rejection of a claim for obviousness in view of a combination of prior art references must be based on a showing of a suggestion, teaching, or motivation that has to be "clear and particular." In re Dembiczak, 175 F.3d at 999. Thus, the mere fact that it is possible to find two isolated disclosures which might be combined to produce a new compound does not necessarily render such production obvious, unless the prior art also suggests the desirability of the proposed combination.

The March 22, 2004 final Office Action failed to establish a *prima facie* case of obviousness because, as the Court in Northern Telecom, Inc. noted, "[i]t is insufficient that the prior art disclosed the components of the patented device" and there is no "teaching, suggestion, or incentive to make the combination." Northern Telecom, Inc.,

908 F.2d at 934. On one hand, the crux of Anand is the formation of a bonding pad formed in a lattice-like shape in which dishing is minimized. Anand specifically points out that dishing is undesirable as "[it] easily causes a bonding error, that is, a wire cannot be bonded to the bonding pad . . . accurately during a wiring bonding operation, which results in the deterioration of the production yield." (Col. 3, lines 18-22). Anand also teaches that the "cavity sections of the lattice-like shape of the bonding pad are filled with the insulating layer" so that "[t]he bonding wire is connected to the lattice-shaped bonding pad." (Abstract). In this manner, with the lattice-like shaped structure, "the bonding error of the device manufactured by the damascening process can be avoided." (Abstract). On the other hand, the crux of Min is the metal-organic atomic-layer deposition of titanium-silicon-nitride films. For this, Min specifically analyzes the "dependence of Si content on the SiH_4 partial pressure" of Ti-Si-N films in both the MOALD and MOCVD methods and concludes that "[t]he MOALD process has a great potential for excellent step coverage due to the complete surface reaction" and that it "demonstrates the perfect step coverage of MOALD." Thus, it is clear that the only element which Anand and Min have in common is the substrate on which their respective structures are formed. Accordingly, a person of ordinary skill in the art would not have been motivated to combine Anand with Min, absent the teachings of the present application.

Appellants also point out that the crux of Anand is not damascene processing. Anand discusses indeed the formation of grooves 19 in the first- and second-level wiring layers, which would arguably correspond to the damascene structure of the claimed invention. However, Anand addresses the formation of grooves 19 only to provide background information for the subsequent formation of the bonding pad with a lattice-like shape over the second-level wiring layer (which is the crux of Anand) and to address bonding errors, and not to provide improved methods of forming damascene structures, much less copper damascene structures.

In view of the above, there is no teaching or suggestion in either of these two references, either independently or combined, of the claimed subject matter and reversal of the rejection of claims 19, 21, 22, 24, 25, 28 and 30 is respectfully requested.

B. CLAIMS 20, 23 AND 40-42 ARE PATENTABLE OVER ANAND AND MIN AND FURTHER IN VIEW OF VENKATRAMAN ET AL. (U.S. PATENT NO. 6,093,966)

Claims 20, 23 and 40-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand and Min and further in view of Venkatraman et al. (U.S. Patent No. 6,093,966) ("Venkatraman"). The final Office Action asserts that although Anand and Min "do not teach that the insulating layers may be formed of polyimide," "Venkatraman et al teach that an insulating layer may be formed of silicon dioxide or polyimide (col. 4, lines 39-54)." (March 22, 2004 Office Action at 3). The Office Action also asserts that "Anand, Min and Venkatraman et al are combinable because they are from the same field of endeavor." (March 22, 2004 Office Action at 3). The Office Action concludes that "[a]t the time of the invention it would have been obvious to a person of ordinary skill in the art to use polyimide as the insulator of Anand." (March 22, 2004 Office Action at 3).

As noted above, the claimed invention relates to a damascene structure having a via lined with a titanium-silicon-nitride layer and filled with copper. As such, independent claim 19 recites a "dual damascene structure" comprising *inter alia* a metal layer provided within a first insulating layer, "a second insulating layer provided over said metal layer" and "a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material." Independent claim 19 also recites a trench situated within a third insulating layer and "lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material."

Claims 20 and 23 depend on independent claim 19 and recite that each of the second insulating layer (claim 20) and the third insulating layer (claim 23) "includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS."

Independent claim 40 recites "a damascene structure" which is part of a processor-based system and which comprises *inter alia* "a metal layer provided within a first insulating layer" and "at least another insulating layer provided over said metal layer, said first insulating layer and said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsequioxane and NANOGLASS." Independent claim 40 also recites "an etch stop layer provided between said first insulating layer and said at least another insulating layer" and "at least one opening situated within said at least another insulating layer and . . . lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper."

Independent claim 42 recites a "damascene structure" comprising *inter alia* "a first insulating layer," "a metal layer provided within said first insulating layer" and "at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS." Independent claim 42 also recites "an etch stop layer provided over and in contact with said at least another insulating layer" and "at least one opening situated within said at least another insulating layer and said etch stop layer, and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material."

Venkatraman relates to "a semiconductor device having a copper barrier layer." (Col. 1, lines 7-8). Venkatraman teaches a copper barrier layer formed when the substrate

is "biased by a first stage bias followed by a second stage bias to accelerate the plasma to the substrate . . . where the first stage bias is less than the second stage bias." According to Venkatraman, the "copper barrier layer 200 is typically a tantalum silicon nitride layer, but may be composed of any combination of refractory metal . . . together with silicon and nitrogen" and "is deposited on the second oxide layer 190 and the insulating layer 180 and along the sidewalls of the opening 195 and 196." (Col. 5, lines 20-26; Fig. 7).

The subject matter of claims 20, 23 and 40-42 would not have been obvious over Anand and Min in view of Venkatraman. Again, the final Office Action fails to establish a *prima facie* case of obviousness. None of Anand, Min and Venkatraman, whether considered alone or in combination, teaches or suggests all limitations of claims 20, 23 and 40-42. As discussed above, Anand and Min fail to teach or suggest a "dual damascene structure" comprising *inter alia* "a via situated within said second insulating layer . . . said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material," as independent claim 19 recites. Venkatraman also fails to teach or suggest "an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100%," as independent claim 19 recites. Venkatraman discloses a copper barrier layer that is "typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, titanium, vanadium together with silicon and nitrogen"(col. 5, lines 22-26), and not the limitations of the claimed invention.

Anand, Min and Venkatraman, whether considered alone or in combination, also fail to disclose, teach or suggest an "insulating layer" that includes "a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS," and "an etch stop layer" provided "between said first insulating layer and said at least another insulating layer" (claim 40) or "over and in contact with said . . . insulating layer" (claim 42). Anand teaches that "an insulating film (borophospho silicate glass (BPSG) or the like) 15 . . . is formed on the transistor" (col.

11, lines 36-39; fig. 27) and that "insulating layer 25 is made of, for example, silicon oxide" (col. 11, line 44; Fig. 28), and not of the materials recited in independent claims 40 and 42. In addition, Min and Venkatraman are silent about elements of a damascene structure, much less about a "damascene structure" comprising an "insulating layer" that includes "a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS" and "an etch stop layer," as recited in independent claims 40 and 42.

Appellants also submit that a person of ordinary skill in the art would not have been motivated to combine the teachings of Anand with those of Min, much less the teachings of Anand with those of Min and Venkatraman. As explained in detail above, Anand addresses bonding pad formation in a lattice-like shape to minimize dishing, whereas Min teaches the metal-organic atomic-layer deposition of titanium-silicon-nitride films. Accordingly, a person of ordinary skill in the art would not have been motivated to combine Anand with Min. In addition, Appellants submit that the crux of Venkatraman is a copper barrier layer formed when the substrate is "biased by a first stage bias followed by a second stage bias to accelerate the plasma to the substrate . . . where the first stage bias is less than the second stage bias." Thus, a person of ordinary skill in the art would not have been motivated to combine Anand (which teaches a bonding pad formed in a lattice-like shape to minimize dishing) with Min (which analyzes the "dependence of Si content on the SiH_4 partial pressure" of Ti-Si-N films in both the MOALD and MOCVD methods) and further with Venkatraman (which teaches a copper barrier layer formed by subjecting a substrate to a first stage bias followed by a second stage bias to accelerate the plasma to the substrate).

For at least these reasons, Anand, Min and Venkatraman, considered alone or in combination, do not disclose, teach or suggest all limitations of claims 20, 23 and 40-42. Reversal of the rejection of these claims is also respectfully requested.

C. CLAIMS 26 AND 27 ARE PATENTABLE OVER ANAND AND MIN AND FURTHER IN VIEW OF REID ET AL. (*Ti-Si-N DIFFUSION BARRIERS BETWEEN SILICON AND COPPER)*

Claims 26 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand and Min and further in view of Reid et al., *Ti-Si-N Diffusion Barriers Between Silicon and Copper*, IEEE Electron Devices Lettrs., Vol. 15, No. 8, pp. 298-300 (1994) ("Reid"). The final Office Action asserts that, although "Anand and Min . . . did not teach that the Ti-Si-N liner layer is between 50-200 Å thick or specifically 100 Å," "Reid et al teach . . . that a layer of Ti-Si-N may be formed at a thickness of 10 nm (100 Å)." (March 22, 2004 Office Action at 3). Thus, the final Office Action concludes that "it would have been obvious to combine Reid et al. with Anand and Min et al to obtain the invention of claims 26 and 27." (March 22, 2004 Office Action at 4).

Claims 26 and 27 depend on independent claim 19 and recite that the titanium-silicon-nitride layer has a thickness "of about 2,000 to 15,000 Angstroms" (claim 26) and "of about 100 Angstroms" (claim 27).

Reid relates to thin films of Ti-Si-N that are sputtered from a Ti_5Si_3 target and formed as diffusion barriers between silicon substrates and copper overlayers. Reid emphasizes that "$Ti_{34}Si_{23}N_{43}$ thin films are exceptional diffusion barriers between silicon and copper" and that "100 nm and 10 nm films are able to prevent copper from reaching the silicon." (Page 299, second column, last paragraph).

Anand, Min and Reid, considered alone or in combination, fail to disclose, teach or suggest all limitations of independent claim 19 and of dependent claims 26 and 27. As discussed above, Anand fails to teach or suggest a "via being lined with an *organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100%* and filled with a copper material," as independent claim 19 recites (emphasis added). Min is also silent about a dual damascene structure, much less about a "dual damascene structure"

having a metal layer provided within a first insulating layer, "a second insulating layer provided over said metal layer" and "a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material," as in the claimed invention.

Similarly, Reid fails to disclose, teach or suggest a "via being lined with an *organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100%* and filled with a copper material," as independent claim 19 recites (emphasis added). Reid teaches that "$Ti_{34}Si_{23}N_{43}$ thin films are exceptional diffusion barriers between silicon and copper" and that "100 nm and 10 nm films are able to prevent copper from reaching the silicon." (Page 299, second column, last paragraph). Reid also teaches, however, that Ti-Si-N thin film "depositions were made by rf-sputtering in a chamber" (page 298, first column, second paragraph), and not by organo-metallic-atomic deposition, as in the claimed invention. As known in the art, deposition by ALD provides improved step coverage over deposition by sputtering, which is particularly important for the Ti-Si-N diffusion barrier deposited on the sidewalls of vias and trenches. Therefore, the product of "organo-metallic-atomic deposited titanium-silicon-nitride layer" is not taught or suggested by Anand, Min or Reid.

Appellants further submit that a person of ordinary skill in the art would not have been motivated to combine the teachings of Anand with those of Min, much less the teachings of Anand with those of Min and Reid. As explained in detail above, Anand addresses bonding pad formation in a lattice-like shape to minimize dishing, whereas Min teaches the metal-organic atomic-layer deposition of titanium-silicon-nitride films. Accordingly, there is no motivation for a person of ordinary skill in the art to combine Anand with Min. In addition, Appellants submit that the crux of Reid is the formation of $Ti_{34}Si_{23}N_{43}$ thin films as diffusion barriers between silicon and copper. Thus, a person of ordinary skill in the art would not have been motivated to combine Anand (which teaches a bonding pad formed in a lattice-like shape to minimize dishing) with Min (which analyzes

the "dependence of Si content on the SiH_4 partial pressure" of Ti-Si-N films in both the MOALD and MOCVD methods) and further with Reid (which teaches a barrier layer of $Ti_{34}Si_{23}N_{43}$ formed between silicon and copper).

Since Anand, Min and Reid do not teach or suggest all the limitations of independent claim 19, and since there is no motivation to combine Anand with Min, and much less Anand with Min and Reid, to attain the subject matter of claims 26 and 27, these claims would not have been obvious over Anand and Min in view of Reid. Accordingly, reversal of the rejection of these claims is also respectfully requested.

D. CLAIMS 31, 33, 34, 37 AND 39 ARE PATENTABLE OVER ANAND IN VIEW OF VENKATRAMAN AND REID

Claims 31, 33, 34, 37 and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand in view of Venkatraman and Reid. The final Office Action asserts that, although "Anand . . . does not teach a polyimide insulator or a Ti-Si-N layer with a thickness of about 100 Å," "Venkatraman makes obvious the use of polyimide and Reid makes obvious the thickness of 100 Å." (March 22, 2004 Office Action at 4).

As noted above, the claimed invention relates to a damascene structure having a via lined with a titanium-silicon-nitride layer and filled with copper. As such, independent claim 31 recites "a damascene structure" comprising *inter alia* a metal layer "provided within" a first insulating layer, "at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS." Independent claim 31 also recites "at least one opening situated within said at least another insulating layer . . . being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material."

Claims 33, 34, 37 and 39 depend on independent claim 31 and recite that the "at least another insulating layer includes silicon dioxide" (claim 33) and "has a thickness of about 2,000 to 15,000 Angstroms" (claim 34). Claim 37 recites that the copper material "includes copper or copper alloy." Claim 39 recites that the substrate is a "silicon substrate."

None of Anand, Venkatraman and Reid, whether considered alone or in combination, discloses, teaches or suggests an "insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS" and "at least one opening situated within said at least another insulating layer . . . being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material," as independent claim 31 recites. Anand teaches that "an insulating film (borophospho silicate glass (BPSG) or the like) 15 . . . is formed on the transistor" (col. 11, lines 36-39; fig. 27) and that "insulating layer 25 is made of, for example, silicon oxide" (col. 11, line 44; Fig. 28), and not of the materials recited in independent claim 31.

Venkatraman also fails to teach or suggest the limitations of independent claim 31. Venkatraman discloses a copper barrier layer that is "typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, titanium, vanadium together with silicon and nitrogen." (Col. 5, lines 22-26). Venkatraman fails to teach or suggest, however, "a titanium-silicon-nitride layer having a thickness of about 100 Angstroms," as independent claim 31 recites. Venkatraman also fails to disclose, teach or suggest the materials of the insulating layer as recited in independent claim 31. Venkatraman teaches an insulating layer including only "organic thermoplastic and thermosetting polymers such as polyimides, polyarylethers, benzocyclobutenes, polyphenylquinoxalines, polyquinolines . . . and polymers of polysiloxane" (Col. 4, lines 42-53).

Further, Reid fails to teach or suggest the insulating materials recited in independent claim 31. Reid teaches only that "$Ti_{34}Si_{23}N_{43}$ thin films are exceptional diffusion barriers between silicon and copper," that "100 nm and 10 nm films are able to prevent copper from reaching the silicon" (page 299, second column, last paragraph), and that Ti-Si-N thin film "depositions were made by rf-sputtering in a chamber." (Page 298, first column, second paragraph). However, Reid fails to disclose, teach or suggest any of the materials recited in independent claim 31, much less "at least one opening situated within said at least another insulating layer . . . being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material," as in the claimed invention.

Appellants submit that a person of ordinary skill in the art would also not have been motivated to combine the teachings of Anand with those of Venkatraman and Reid. As detailed above, Anand addresses bonding pad formation in a lattice-like shape to minimize dishing. In contrast, Venkatraman addresses the formation of a copper barrier layer by subjecting a substrate to a first stage bias followed by a second stage bias to accelerate the plasma to the substrate, while Reid teaches the formation of a barrier layer of $Ti_{34}Si_{23}N_{43}$ between silicon and copper. Accordingly, the only element which Anand, Venkatraman and Reid have in common is a substrate on which their respective structures are formed. Thus, a person of ordinary skill in the art would not have been motivated to combine Anand with Venkatraman and Reid. For at least these reasons, the final Office Action fails again to establish a *prima facie* case of obviousness and reversal of the rejection of claims 31, 33, 34, 37 and 39 is respectfully requested.

In conclusion, Appellants respectfully submit that the final rejection of claims 19-28, 30, 31, 33, 34, 37 and 39-42 is in error for at least the reasons outlined above. Reversal of the final rejection of claims 19-28, 30, 31, 33, 34, 37 and 39-42 is requested.

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Respectfully submitted,

By_____

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VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached below:

19. A dual damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

a second insulating layer provided over said metal layer;

a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material;

a third insulating layer located over said second insulating layer;

a trench situated within said third insulating layer and extending to said via, said trench being lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material.

20. The dual damascene structure of claim 19, wherein said second insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

21. The dual damascene structure of claim 19, wherein said second insulating layer includes silicon dioxide.

22. The dual damascene structure of claim 19, wherein said second insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

23. The dual damascene structure of claim 19, wherein said third insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

24. The dual damascene structure of claim 19, wherein said third insulating layer includes silicon dioxide.

25. The dual damascene structure of claim 19, wherein said third insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

26. The dual damascene structure of claim 19, wherein said titanium-silicon-nitride layer has a thickness of about 2,000 to 15,000 Angstroms.

27. The dual damascene structure of claim 19, wherein said titanium-silicon-nitride layer has a thickness of about 100 Angstroms.

28. The dual damascene structure of claim 19, wherein said copper material includes copper or a copper alloy.

30. The dual damascene structure of claim 19, wherein said substrate is a silicon substrate.

31. A damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS; and

at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material.

33. The damascene structure of claim 31, wherein said at least another insulating layer includes silicon dioxide.

34. The damascene structure of claim 31, wherein said at least another insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

37. The damascene structure of claim 31, wherein said copper material includes copper or a copper alloy.

39. The damascene structure of claim 31, wherein said substrate is a silicon substrate.

40. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer provided within a first insulating layer formed over a substrate, at least another insulating layer provided over said metal layer, said first insulating layer and said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS, an etch stop layer provided between said first insulating layer and said at least another insulating layer, and at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper.

41. The processor-based system of claim 40, wherein said processor and said integrated circuit are integrated on same chip.

42. A damascene structure comprising:

a first insulating layer provided over a semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS;

an etch stop layer provided over and in contact with said at least another insulating layer; and

at least one opening situated within said at least another insulating layer and said etch stop layer, and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material.

IX. EVIDENCE APPENDIX

No evidence was submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132 and no evidence was entered in the record by the Examiner.

X. RELATED PROCEEDINGS APPENDIX

As known to Appellants, their legal representative, or the assignee, there are no decisions rendered by a court or by the Board pertaining to appeals, interferences or judicial proceedings related to the pending appeal, or that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.